REMARKS

Claim 1 has been amended to include the subject matter of former dependent claim 7. That claim was rejected under Section 103 over the combination of Arimilli in view of Wu.

It was asserted that Wu discloses performing virtual-to-physical translation in said region, citing column 10, lines 39-41, and column 6, lines 58-59. But this does not seem to be the case since it is explained in column 10, lines 39-41, that it is a translation look aside buffer (TLB) that "is invoked to generate a real address for indexing the L2 cache."

Thus, plainly, it is not the L2 cache that does the address translation. As pointed out in the present application at page 8, lines 22 *et seq.*, in some embodiments, mapping within each L2 cache line of which L1 cache way within each set holds the data in that L2 line serves as a physical-to-virtual address translation. Thus, if two cores were served by the same L2 cache, and each was using different address mapping so that each was accessing the same physical address through two different virtual addresses, both would still be properly updated to maintain cache coherence. In some embodiments, a translation look aside buffer would not be needed in the present invention.

The other claims have been similarly amended and, therefore, it is believed that the application is now in condition for allowance. The Examiner's prompt action in allowance is respectfully requested.

Respectfully submitted,

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